REMARKS

Reconsideration of this application, as amended, is respectfully requested.

Claims 1-6, 8-9 and 11-15 are pending. Claims 1-6, 8-9 and 11-15 stand rejected.

In this response, claims 1, 13, and 15 have been amended. No claims have been canceled. No claims have been added. Support for the amendments is found in the specification, the drawings, and in the claims as originally filed. Applicants respectfully submit that the amendments do not add new matter.

REJECTIONS UNDER 35 U.S.C. § 103

Claims 1, 8, 9 and 11 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,060,033 to Takeuchi ("Takeuchi '033").

Amended claim 1 reads as follows:

> A device comprising:
> a substrate that has a first conductivity region and recesses, wherein the recesses have a first inwardly concaved geometry with first inflection points;
> a gate dielectric formed on the first conductivity region of the substrate between the recesses;
> a gate electrode formed on said gate dielectric, said gate electrode having a lower portion formed directly on said gate dielectric;
> a pair of sidewall spacers formed along laterally opposite sidewalls of said gate electrode; and
> a silicon or silicon alloy layer deposited into the recesses to form a pair of inwardly concaved source/drain regions of a second conductivity type having a concentration of impurities in a range of $1x10^{18}/cm^3$ to $3x10^{21}/cm^3$ on opposite sides of said gate electrode , wherein the source/drain regions have a second inwardly concaved geometry with second inflection points that is determined by the first geometry creating metallurgical inflection points directly beneath said lower portion of said gate electrode formed directly on said gate dielectric layer, wherein said silicon or silicon alloy source/drain regions extend the greatest distance laterally beneath said lower portion of the gate electrode at said inflection points, which occurs between 50-250Å laterally beneath said gate electrode and at a depth of between 25-100Å beneath said gate dielectric, and directly define a first channel region having a first metallurgical channel length directly beneath said lower portion of said gate electrode in said first conductivity type region, and a second channel region having a second metallurgical length between said metallurgical inflection points, wherein said first metallurgical channel length directly beneath said lower portion of said gate

electrode is larger than said second metallurgical channel length between said metallurgical inflection points.

(Amended claim 1) (emphasis added)

Takeuchi'033 discloses a MOS transistor. More specifically, Takeuchi'033 discloses that the transistor has a gate oxide on the substrate (Figures 1d-1h, col. 4, lines 10-16) and source/drain regions with low and high concentration of impurities in the substrate (col. 3, lines 50-67, Figure 1h). In particular, Takeuchi'033 discloses that the source and drain regions are formed by the distribution of the impurities during ion implantation and annealing (col. 3, lines 60-63, col. 4, lines 37- 67Figure 1e).

Thus, Takeuchi'033 merely discloses that the geometry of source and drain regions is determined by the distribution of the impurities. In contrast, amended claim 1 refers to a silicon or silicon alloy layer deposited into the recesses to form a pair of source/drain regions on opposite sides of said gate electrode, wherein the source/drain regions have an inwardly concaved geometry with inflection points that is determined by the geometry of the recesses in the substrate.

Further, Takeuchi'033 merely discloses a gate oxide on the substrate. In contrast, amended claim 1 refers to a gate dielectric that is formed between the recesses in the substrate.

Additionally, Takeuchi'033 fails to disclose, teach, or suggest a substrate that has a first conductivity region and recesses, wherein the recesses have a first inwardly concaved geometry with first inflection points, as recited in amended claim 1.

Therefore, Applicants respectfully submit that amended claim 1 is not obvious under 35 U.S.C. § 103(a) over Takeuchi'033.

Because claims 8, 9, and 11 depend from amended claim 1, and add additional limitations, Applicants respectfully submit that claims 8, 9, and 11 are not obvious under 35 U.S.C. § 103(a) over Takeuchi'033.

Claim 2 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Takeuchi '033 as applied to claims 1, 8, 9 and 11 above, and further in view of U.S. Patent No. 5,970,351 to Takeuchi ("Takeuchi '351").

Takeuchi'351 discloses elevated drain/source regions formed on a substrate, and similarly to also fails to disclose the discussed limitations of amended claim1.

Thus, neither Takeuchi'033, Takeuchi'351, nor any combination thereof discloses a substrate that has a first conductivity region and recesses, wherein the recesses have a first inwardly concaved geometry with first inflection points, as recited in amended claim 1.

Further, neither Takeuchi'033, Takeuchi'351, nor any combination thereof discloses a gate dielectric formed on the first conductivity region of the substrate between the recesses, as recited in amended claim 1. Further, neither Takeuchi'033, Takeuchi'351, nor any combination thereof discloses a silicon or silicon alloy layer deposited into the recesses to form a pair of source/drain regions on opposite sides of said gate electrode, wherein the source/drain regions have a second inwardly concaved geometry with second inflection points that is determined by the first geometry, as recited in amended claim 1.

Therefore, Applicants respectfully submit that claim 2 is not obvious under 35 U.S.C. § 103(a) over Takeuchi'033, in view of Takeuchi'351.

Claim 3 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Takeuchi'033, in view of U.S. Patent No. 6,057,582 to Choi ("Choi '582").

Choi'582 discloses a transistor having a gate insulating film having thicknesses at both sides thicker than a thickness at a center formed on semiconductor substrate 21, and

similarly to Takeuchi'033 and Takeuchi'351, fails to disclose the discussed limitations of amended claim 1.

Furthermore, even if Takeuchi'033 and Choi'582 were combined, such a combination would lack the discussed limitations of amended claim 1. Because claim 3 contains the discussed limitations, Applicants respectfully submit that claim 3 is not obvious under 35 U.S.C. § 103(a) over Takeuchi'033 in view of Choi'582.

Claim 4 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Takeuchi '033, in view of Takeuchi '351 as applied to claim 2 above, and further in view of Choi '582.

As set forth above, neither Takeuchi'033, Takeuchi'351, Choi'582, nor any combination thereof, discloses the discussed limitations of amended claim 1.

Because claim 4 depends from amended claim 1 and add additional limitations, Applicants respectfully submit that claim 4 is not obvious under 35 U.S.C. § 103(a) over Takeuchi'033, in view of Takeuchi'351, and further in view of Choi'582.

Claims 5 and 6 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Takeuchi '033 as applied to claims 1, 8, 9 and 11 above, and further in view of U.S. Patent No. 5,793,088 to Choi et al. ("Choi '088").

Choi'088 discloses controlling the threshold voltage by providing a threshold voltage implant into the edges of the halo regions, and similarly to Takeuchi'033, does not disclose the discussed limitations of amended claim 1.

Because claims 5 and 6 depend from amended claim 1 and add additional limitations, Applicants respectfully submit that claims 5 and 6 are not obvious under 35 U.S.C. § 103(a) over Takeuchi'033, in view of Choi'088.

Claim 12 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Takeuchi '033 as applied to claims 1, 8, 9 and 11 above, and further in view of U.S. Patent No. 5,567,966 to Hwang ("Hwang").

Hwang discloses thinning the channel region by local oxidation and wet etch, and similarly to Takeuchi'033, fails to disclose the discussed limitations of amended claim 1. Thus, neither Takeuchi'033, Hwang, nor a combination thereof, discloses such limitations of amended claim 1.

Because claim 12 depends from amended claim 1, Applicants respectfully submit that claim 12 is not obvious under 35 U.S.C. § 103(a) over Takeuchi'033, in view of Hwang.

Claim 13 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Takeuchi '033 in view of U.S. Patent No. 6,274,894 to Wieczorek et al. ("Wieczorek") in view of Takeuchi '351.

Wieczorek discloses forming low-bandgap source and drain regions for MOS transistors, and similarly to Takeuchi'033 and Takeuchi'351, fails to disclose the discussed limitations.

Because claim 13 contains the discussed limitations, Applicants respectfully submit that claim 13 is not obvious under 35 U.S.C. § 103(a) over Takeuchi'033, in view of Wieczorek, and further in view of Takeuchi'351.

Claim 14 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Takeuchi '033 in view of Wieczorek in view of Takeuchi '351 as applied to claim 13 above, and further in view of Choi '582.

As set forth above, neither Takeuchi'033, Wieczorek, Takeuchi'351, Choi'582, nor a combination thereof, discloses the discussed limitations.

Because claim 14 depends from amended claim 13, Applicants respectfully submit that claim 14 is not obvious under 35 U.S.C. § 103(a) over Takeuchi'033, in view of Wieczorek, in view of Takeuchi'351, and further in view of Choi'582.

Claim 15 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Takeuchi '033 in view of Wieczorek.

As set forth above, neither Takeuchi'033, Wieczorek, nor a combination thereof, discloses the discussed limitations.

Because amended claim 15 contains the discussed limitations, Applicants respectfully submit that amended claim 15 is not obvious under 35 U.S.C. § 103(a) over Takeuchi'033, in view of Wieczorek.

CONCLUSION

It is respectfully submitted that in view of the amendments and arguments set forth herein, the applicable rejections and objections have been overcome. If there are any additional charges, please charge Deposit Account No. 02-2666 for any fee deficiency that may be due.

Respectfully submitted,

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